CLAIMS

What is claimed is:

1. A method of forming an isolation structure for a semiconductor device, comprising:

providing a semiconductor substrate having a first surface and a second surface;

patterning at least one first doped area on said substrate first surface;

forming a layer of oxide over said substrate first surface;

depositing a diffusion barrier layer over said pad oxide layer; and

annealing said substrate to activate said at least one first doped area after deposition of diffusion barrier.

2. The method of claim 1, wherein depositing said diffusion barrier layer over said pad oxide layer includes depositing said diffusion barrier layer over said substrate second surface.

3. The method of claim 1, further comprising depositing a second diffusion barrier layer over said substrate second surface.

4. The method of claim 1, wherein said first doped area comprises a p-type impurity.

5. The method of claim 1, wherein said first doped area comprises an n-type impurity.

6. The method of claim 1, wherein said diffusion barrier layer is silicon nitride.

7. The method of claim 1, wherein said diffusion barrier layer is silicon oxynitride.

8. The method of claim 1, further comprising:

applying a mask material over said diffusion barrier;

etching said diffusion barrier to define at least one active device area comprised of said at least one activated first doped area;

stripping said mask material;

growing a field oxide from said pad oxide layer; and

removing said diffusion barrier and a portion of said field oxide to expose portions of said substrate first surface.

9. A method of forming a MOS structure, comprising:

providing a semiconductor substrate having a first surface and a second surface;

patterning at least one first doped area on said substrate first surface;

forming a layer of oxide over said substrate first surface;

depositing a diffusion barrier layer over said pad oxide layer; and

annealing said substrate to activate said at least one first doped area after deposition of diffusion barrier.

10. The method of claim 9, wherein depositing said diffusion barrier layer over said pad oxide layer includes depositing said diffusion barrier layer over said substrate second surface.

11. The method of claim 9, further comprising depositing a second diffusion barrier layer over said substrate second surface.

12. The method of claim 9, wherein said first doped area comprises a p-type impurity.

13. The method of claim 9, wherein said first doped area comprises an n-type impurity.

14. The method of claim 9, wherein said diffusion barrier layer is silicon nitride.

15. The method of claim 9, wherein said diffusion barrier layer is silicon oxynitride.

16. The method of claim 9, further comprising:

applying a mask material over said diffusion barrier;

etching said diffusion barrier to define at least one active device area comprised of said at least one activated first doped area;

stripping said mask material;

growing a field oxide from said oxide layer; and

removing said diffusion barrier and a portion of said field oxide to expose portions of said substrate first surface.

17. A well-drive anneal technique using preplacement of nitride films for enhanced field isolation, comprising:

providing a semiconductor substrate having a first surface and a second surface;

patterning at least one first doped area on said substrate first surface;

forming a layer of oxide over said substrate first surface;

depositing a diffusion barrier layer over said pad oxide layer; and

annealing said substrate to activate said at least one first doped area after deposition of diffusion barrier.

18. The technique of claim 17, wherein depositing said diffusion barrier layer over said pad oxide layer includes depositing said diffusion barrier layer over said substrate second surface.

19. The technique of claim 17, further comprising depositing a second diffusion barrier layer over said substrate second surface.

20. The technique of claim 17, wherein said first doped area comprises a p-type impurity.

21. The technique of claim 17, wherein said first doped area comprises an n-type impurity.

22. The technique of claim 17, wherein said diffusion barrier layer is silicon nitride.

23. The technique of claim 17, wherein said diffusion barrier layer is silicon oxynitride.

24. The technique of claim 17, further comprising:

applying a mask material over said diffusion barrier;

etching said diffusion barrier to define at least one active device area comprised of said at least one activated first doped area;

stripping said mask material;

growing a field oxide from said oxide layer; and

removing said diffusion barrier and a portion of said field oxide to expose portions of said substrate first surface.

25. A pre-anneal intermediate structure in the formation of an isolation structure for a semiconductor device, comprising:
a semiconductor substrate having a first surface and a second surface;
at least one first doped area on said substrate first surface; and
a diffusion barrier layer over said substrate first surface.

26. The structure of claim 25 further comprising a layer of oxide between said substrate first surface and said diffusion barrier layer.

27. The structure of claim 25 wherein said diffusion barrier layer extends over said substrate second surface.

28. The structure of claim 25, further comprising a second diffusion barrier layer over said substrate second surface.

29. The structure of claim 25, wherein said first doped area comprises a p-type impurity.

30. The structure of claim 25, wherein said first doped area comprises an n-type impurity.

31. The structure of claim 25, wherein said diffusion barrier layer is silicon nitride.

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32. The structure of claim 25, wherein said diffusion barrier layer is silicon oxynitride.

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